



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,485	02/27/2004	Thilo Stolze	074313.0105	7994
7590 09/17/2008				
Andreas Grubert Baker Botts L.L.P. One Shell Plaza 910 Louisiana Houston, TX 77002-4995			EXAMINER ARENA, ANDREW OWENS	
			ART UNIT 2811	PAPER NUMBER
			MAIL DATE 09/17/2008	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

**Application No.**

10/789,485

**Applicant(s)**

STOLZE, THILO

**Examiner**

Andrew O. Arena

**Art Unit**

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 30 June 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,3-5,8,9,11-14 and 17-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 3-5, 8, 9, 11-14 and 17-24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB008)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

A request for continued examination, for which this application is eligible, under 37 CFR 1.114, including timely payment of the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. The submission of 06/30/2008 has been entered.

### ***Response to Arguments***

The arguments filed 6/20/2008 were fully considered but they are not persuasive.

The argument that "Ali fails to teach or suggest both... ..features" (pg 7 of 9, ¶12) is not convincing since (turning to Ali Fig 4) everything which surrounds the discrete parts 14, 16, 18, 80, 82, 60 and 62 may be regarded as the claimed "module housing". Therefore, connecting elements 20 are part of the housing and have recesses therein, further, the language "extending from an exterior" must be interpreted per MPEP § 2111 and does not require a structure different from Ali; e.g., the recess can be regarded as extending from an exterior portion (12), or from but not directly contacting the outside.

### ***Claim Objections***

Claims 3, 5, 8, 9, 11, 12, 17, 19 and 21 are objected to under 37 CFR § 1.75(c) as being of improper dependent form since the claims do not refer back to any pending claim. It is clear that the referred cancelled claims are now incorporated into respective independent claims, from which the objected claims will be treated as depending from.

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1, 3, 8, 9, 12-14 and 19-24 are rejected under 35 U.S.C. § 102(b) as being anticipated by Ali (US 6,157,538)

**RE claim 1**, Ali discloses (e.g., Fig 4) a power semiconductor module (e.g., col 2 ln 31-51) comprising a plurality of semiconductor components (14, 16, 18; col 3 ln 25) situated on substrate regions (60, 62), wherein:

each substrate region (60, 62) has a top surface and side faces, wherein side faces of two adjacent substrate regions face each other;

between each two adjacent substrate regions a connecting element (20) is arranged such that the connecting element directly contacts the side faces of the two adjacent substrates, wherein said connecting elements are designed to prevent a deformation of one substrate region to continue to an adjacent substrate region (Ali discloses claimed structure, capable of claimed function, see MPEP § 2114); and

wherein the connecting regions are formed by recesses in a module housing (the enclosure in Fig 4) enclosing said substrate portions,

each recess extending from an exterior (per MPEP § 2111) of the housing.

**RE claim 3**, Ali discloses the material recesses are slotted.

**RE claims 8, 9 & 12**, Ali discloses the module housing, at least in the regions of the substrate regions, is such that it acts on the substrate regions with a spring force (solids have inherent elastic modulus, and exert a spring force upon contact).

**RE claim 13**, Ali discloses (Fig 3) the power semiconductor module has a housing (11), which, in an area between the substrate regions, has action points (where 20 contacts 60/62) for a mechanical pressure application of the connecting regions, and the housing applies pressure to the individual substrate regions.

**RE claim 14**, Ali discloses (e.g., Fig 4) a power semiconductor module (e.g., col 2 ln 31-51) comprising:

a plurality of substrate elements (60, 62) having a top and bottom surface and sidewalls, each substrate element comprising a semiconductor component (14, 16, 18) arranged on the top surface of a substrate element;

one or a plurality of connecting regions (20) directly contacting opposing sidewalls of two adjacent substrate elements, wherein said connecting elements are designed to prevent a deformation of one substrate region to continue to an adjacent substrate region (Ali discloses claimed structure, capable of claimed function, see MPEP § 2114);

a module housing (enclosure of Fig 4) enclosing said plurality of substrate elements; and

wherein the connecting elements are formed by recesses in the module housing extending from an exterior (per MPEP § 2111) an exterior of the housing.

**RE claim 15**, Ali discloses a module housing (11) enclosing said plurality of substrate elements.

**RE claim 16**, Ali discloses the connecting elements are formed by recesses.

**RE claim 17**, Ali discloses the material recesses are slotted.

**RE claim 19**, Ali discloses the module housing, at least in the regions of the substrate regions, is such that it acts on the substrate regions with a spring force (solids have inherent elastic modulus, and exert a spring force upon contact).

**RE claims 20 & 22**, Ali discloses a heat sink (66; col 3 ln 51) having a flat (top) surface, wherein a bottom surface of the plurality of substrate elements (60, 62) and said plurality of connecting regions are arranged on said flat surface.

**RE claim 21**, Ali discloses the module housing (32) in a region between the substrate elements comprises action points (where 20 contacts 60/62) for a mechanical pressure application of the connecting elements, and the housing applies pressure to the individual substrate regions (ln 5-6).

**RE claim 23**, Ali discloses (e.g., Fig 4) a power semiconductor module (e.g., col 2 ln 31-51) comprising:

- a heat sink (66; col 3 ln 51) having a flat (top) surface;
- a plurality of substrates (60, 62) arranged on the flat surface of the heat sink;
- a plurality of semiconductor components (14, 16, 18) arranged on the substrates;
- one or a plurality of connecting regions (20) in direct contact with adjacent ones of the substrates and arranged directly on the flat surface of the heat sink between adjacent ones of the substrates, wherein
- the connecting regions are formed by recesses in a module housing (enclosure) enclosing said substrate regions,
- each recess extending from an exterior of the housing.

**RE claim 24**, Ali discloses (e.g., Fig 4) a power semiconductor module (e.g., col 2 ln 31-51), comprising:

a substrate segmented into a plurality of spaced apart substrate regions (60,62) ;  
at least one semiconductor component (14, 16, 18) arranged on one or more of the substrate regions;

a connecting region (20) arranged in the space between adjacent ones of the substrate regions; and

wherein the connecting region forms an articulated hinge with each of the adjacent substrate regions so that the adjacent substrate regions can move relative to one another about the articulated hinges (Ali capable of this function; MPEP § 2114).

### ***Claim Rejections - 35 USC § 103***

Claims 4, 5, 11 and 18 are rejected under 35 U.S.C. § 103(a) as obvious over Ali as applied to claims 1, 2, and 14 above, in view of Mikio (JP Pub 2001-118987).

**RE claims 4, 5 & 18**, Ali differs from the claimed invention only in not expressly disclosing the substrate is a ceramic.

Mikio discloses an analogous device on a ceramic substrate.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that in Ali, in view of Mikio, the substrate regions are ceramic; at least for high heat dissipation (JPO machine translation of Mikio: ¶13).

**RE claim 11**, Ali discloses (Fig 3) the module housing, at least in the regions of the substrate regions, is such that it acts on the substrate regions with a spring force (solids have inherent elastic modulus, and exerts a spring force on contact).

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is (571)272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571- 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. For more info about PAIR, see <http://pair-direct.uspto.gov>. For questions PAIR access, contact the Electronic Business Center at 866-217-9197 (toll-free). For assistance from a USPTO Customer Service Rep or access to the automated info system, call 800-786-9199 or 571-272-1000.

/Andrew O. Arena/  
Examiner, Art Unit 2811  
14 September 2008

/Lynne A. Gurley/  
Supervisory Patent Examiner, Art  
Unit 2811